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TITLE: Superconductor-semiconductor hybrid memory circuits with superconducting three-terminal switching devices
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INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ghoshal; Uttam S.	Austin	TX	N/A	N/A
Kroger; Harry	Austin	TX	N/A	N/A

US-CL-CURRENT: 365/162; 365/161, 365/177, 365/182, 369/145, 505/170, 505/193, 505/834 , 505/837, 505/841

CLAIMS:

What is claimed is:
1. A memory cell for storing and accessing information in binary form of the type useful in computer or logic circuits applications wherein a matrix comprised of a plurality of memory cells of common design is formed in row and column format, with rows being addressed via word-lines and columns being addressed via bit-lines, said cell comprising:
(a) a word-line input terminal;
(b) a bit-line input terminal;
(c) a first superconducting voltage controlled, three-terminal switching device, and a second superconducting voltage controlled, three-terminal switching device, each of said switching devices having a gate voltage terminal and first and second pass terminals, wherein the current flowing through each switching device via said pass terminals is controlled by the voltage applied to said gate terminal;
(d) a semiconductor charge storing circuit for storing charge representing information in binary form, said semiconductor charge storing circuit having at least a first and a second output terminal; and
(e) a superconducting current sensing means, said current sensing means having a biased current circuit with a bias input and a bias output, and a sensed current circuit with

a sensed current input and a sensed current output;
wherein said first pass terminal of said first switching device is connected to said word-line terminal;
said gate terminal of said first switching device is connected to said first output terminal of said semiconductor charge storing circuit;
said second pass terminal of said first switching device is connected to said sensed current input;
said first pass terminal of said second switching device is connected to said word-line terminal;
said gate terminal of said second switching device is connected to said second output terminal of said semiconductor charge storing circuit;
said second pass terminal of said second switching device is connected to said sensed current output; and
said bias input is connected to said bit-line input terminal.

2. The memory cell of claim 1, wherein said semiconductor charge storing circuit is a logic circuit being of a type that the output voltage on said first and second output terminals are logic complements.

3. The memory cell of claim 1, wherein said semiconductor charge storing circuit is a bi-stable logic circuit being of a type that the output voltage of said first and second output terminals are logic complements.

4. The memory cell of claim 1, wherein said first and second superconducting switch devices each comprise a superconducting field-effect transistor having a superconducting source, a superconducting drain, a conducting gate, and a semiconducting channel, and wherein the drain to source current is controlled by the applied gate to source voltage.

5. The memory cell of claim 1, wherein said superconducting current sensing means comprises a superconducting field-effect transistor having a superconducting source, a superconducting drain, a conducting gate, and a semiconducting channel, and wherein the drain is the sensed current input and the source is the sensed current output, and wherein the bias input is connected to said bit line and to said drain, and the bias output is connection to said source.

6. The memory cell of claim 1, wherein said superconducting current sensing means comprises a superconducting quantum interference device.

7. A memory cell for storing and accessing information in binary form of the type useful in computer or logic circuits applications wherein a matrix comprised of a plurality of memory cells of common design is formed in row and column format, with rows being addressed via word-lines and columns being addressed via bit-lines, said cell comprising:

(a) a word-line input terminal;

(b) a bit-line input terminal;

(c) a first superconducting voltage controlled, three-terminal switching device, and a second superconducting voltage controlled, three-terminal switching device, each of said switching devices having a

gate voltage terminal and first and second pass terminals wherein the current flowing through each switching device via said pass terminals is controlled by the voltage applied to said gate terminal, the current flow through said first switching device being biased by a gate terminal voltage the logic complement of the gate terminal voltage needed to bias current flow through said second switching device;
(d) A gate terminal voltage creation means for actuating said switching devices having at least an output terminal;

(e) a superconducting current sensing means, said current sensing means having a biased current circuit with a bias input and a bias output, and a sensed current circuit with a sensed current input and a sensed current output;
wherein said first pass terminal of said first switching device is connected to said word-line terminal;
said gate terminal of said first switching device is connected to said output terminal of said voltage creation means;
said second pass terminal of said first switching device is connected to said sensed current input;
said first pass terminal of said second switching device is connected to said word-line terminal;
said gate terminal of said second switching device is connected to said output terminal of said voltage creation means;
said second pass terminal of said second switching device is connected to said sensed current output; and
said bias input is connected to said bit-line input terminal.
8. The memory cell of claim 7, wherein said first superconducting switch device comprises a superconducting field-effect transistor having a superconducting source, a superconducting drain, a conducting gate, and a n-doped semiconducting channel, and said second superconducting switch device comprises a superconducting field-effect transistor having a superconducting source, a superconducting drain, a conducting gate, and a p-doped semiconducting channel, wherein the drain to source current of said first switch device is biased by an applied gate to source voltage which is the logic complement of the applied gate to source voltage needed to bias the drain to source current of the second switching device.
9. The memory cell of claim 7, wherein said superconducting current sensing means comprises a superconducting field-effect transistor having a superconducting source, a superconducting drain, a conducting gate, and a semiconducting channel, and wherein the drain is the sensed current input and the source is the sensed current output, and wherein the bias input is connected to said bit line and to said drain, and the bias output is connected to said source.
10. The memory cell of claim 7, wherein said superconducting current sensing means comprises a superconducting quantum interference device.

11. The memory cell of claim 7, wherein said gate voltage creation means comprises a semiconducting field effect transistor having a semiconducting source, a semiconducting drain, a conducting gate, and a semiconducting channel, wherein the drain to source current is controlled by the applied gate to source voltage, and wherein said source is the output terminal of said gate voltage creation means.

12. A memory cell for storing and accessing information in binary form of the type useful in computer or logic circuits applications wherein a matrix comprised of a plurality of memory cells of common design is formed in row and column format, with rows being addressed via word-lines and columns being addressed via bit-lines, said cell comprising:

(a) a word-line input terminal;

(b) a bit-line input terminal;

(c) a superconducting voltage controlled, three-terminal switching device, said switching device having a gate voltage terminal and first and second pass terminals wherein the current flowing through said switching device via said pass terminals is controlled by the voltage applied to said gate terminal;

(d) an inductor means having an input terminal and an output terminal;

(e) a gate terminal voltage creation means for actuating said switching device having at least an output terminal;

(f) a superconducting current sensing means, said current sensing means having a biased current circuit with a bias input and a bias output, and a sensed current circuit with a sensed current input and a sensed current output;

wherein said first pass terminal of said switching device is connected to said word-line terminal;

said gate terminal of said switching device is connected to said voltage creation means;

said second pass terminal of said switching device is connected to said sensed current input;

said input terminal of said inductor means is connected to said word-line terminal;

said output terminal of said inductor means is connected to said sensed current output; and

said bias input is connected to said bit-line input terminal;

13. The memory cell of claim 12, wherein said inductor means is a superconducting inductor.

14. The memory cell of claim 12, wherein said inductor means is a metallic inductor.

15. The memory cell of claim 12, wherein said superconducting switch device comprises a superconducting field-effect transistor having a superconducting source, a superconducting drain, a conducting gate, and a superconducting channel, and wherein the drain to source current is controlled by the applied gate to source voltage.

16. The memory cell of claim 12, wherein said superconducting current sensing means comprises a superconducting field-effect transistor having a

superconducting source, a superconducting drain, a conducting gate, and a semiconducting channel, and wherein the drain is the sensed current input and the source is the sensed current output, and wherein the bias input is connected to said bit line and to said drain, and the bias output is connection to said source.

17. The memory cell of claim 12, wherein said superconducting current sensing means comprises a superconducting quantum interference device.

18. A memory cell for storing and accessing information in binary form of the type useful in computer or logic circuits applications wherein a matrix comprised of a plurality of memory cells of common design is formed in row and column format, with rows being addressed via word-lines and columns being addressed via bit-lines, said cell comprising:

(a) a word-line input terminal;

(b) a bit-line input terminal;

(c) a first semiconducting voltage controlled, three-terminal switching device, said switching device having a gate voltage terminal and first and second pass terminals wherein the current flowing through said switching device via said pass terminals is controlled by the voltage applied to said gate terminal;

(d) a capacitance means having at least a first terminal and a second terminal; and

(e) a superconducting current sensing means, said current sensing means having a biased current circuit with a bias input and a bias output, and a sensed current circuit with a sensed current input and a sensed current output;

wherein said gate terminal of said switching device is connected to said word-line terminal;

said first pass terminal of said switching device is connected to said bit-line terminal;

said second pass terminal of said switching device is connected to said first terminal of said capacitance means;

said second terminal of said capacitance means is connected to electrical ground; and

said bias input is connected to said bit-line input terminal.

19. The memory cell of claim 18, wherein said capacitance means is the gate to source capacitance of a second semiconducting voltage controlled, three terminal switching device, said switching device having a gate voltage terminal and first and second pass terminals wherein the current flowing through said switching device via said pass terminals is controlled by the voltage applied to gate terminals and wherein said first pass terminal of said second switching device is connected to said second pass terminal of said first switching device, said gate terminal is the first terminal of said capacitance means of said capacitance means and said second terminal is said second pass terminal of said second semiconducting device.

20. The memory cell of claim 18, further comprising a gate terminal voltage creation means having at least an output

terminal, wherein said output terminal is connected to said first terminal of said capacitance means.

21. The memory of claim 18, wherein said gate voltage creation means comprises a semiconducting field effect transistor having a semiconducting source, a semiconducting drain, a conducting gate, and a semiconducting channel, wherein the drain to source current is controlled by the applied gate to source voltage, and wherein said source is the output terminal of said gate voltage creation means.

22. The memory cell of claim 18, wherein said superconducting current sensing means comprises a superconducting field-effect transistor having a superconducting source, a superconducting drain, a conducting gate, and a semiconducting channel, and wherein the drain is the sensed current input and the source is the sensed current output, and wherein the bias input is connected to said bit line and to said drain, and the bias output is connection to said source.

23. The memory cell of claim 18, wherein said superconducting current sensing means comprises a superconducting quantum interference device.

24. The memory cell of claim 18, wherein said superconducting current sensing means comprises a rapid single flux quantum current sensing buffer/amplifier circuit.

25. The memory cell of claim 18, wherein said superconducting current sensing means comprises a superconductor link circuit.

26. The memory cell of claim 18, wherein said current sensing means further comprises a self-timing means comprising a voltage controlled three-terminal switching device having a gate voltage terminal and first and second pass terminals, wherein the current flowing through said switching device via said pass terminals is controlled by the voltage applied to said gate terminal, and wherein said gate terminal is connected to a self-timed signal, said first pass terminal is connected to said bias input and said second pass terminal is connected to said sensed current input.

27. The memory cell of claim 18, further comprising:

a data-in terminal;

a second voltage controlled three-terminal switching device comprising a gate voltage terminal and first and second pass terminals, wherein the current flowing through said switching device via said pass terminals is controlled by the voltage applied to said gate terminal;

a voltage source; and

a superconductor switching device having at least a first and second terminal;

wherein said data-in terminal is connected to said gate terminal of said second switching device;

said first pass terminal is connected to said voltage source;

said second pass terminal of said second switching device is connected to said first terminal of said superconductor switching device;

said second terminal of said superconductor switching device is connected to said first pass terminal of said first switching device.

28. The memory cell of claim 27, wherein said superconductor switching device is a stack of Josephson junction devices.

29. The memory cell of claim 27, wherein said superconductor switching device is a superconducting link.

30. The memory cell of claim 27, wherein said superconductor switching device is voltage controlled superconducting field-effect transistor having a conducting gate, a superconducting source and a superconducting drain, wherein the drain to source current is controlled by the applied gate to source voltage and wherein said gate is connected to said data-in terminal, said drain is connected to said second pass terminal of said second switching device, and said source is connected to said first terminal of said first switching device.

31. A method of accessing from a memory cell having at least a first terminal and a second terminal information in binary forms of the type useful in computer or logic circuit applications, wherein a matrix comprised of a plurality of memory cells of common design is formed in a row and column format, with rows being addressed via word lines, wherein each word line is connected to said first terminal of each memory cell in said row, and columns being addressed via bit-lines, wherein a superconducting current sensing means having a biased current circuit with a bias input and a bias output, and a sensed current circuit with a sensed current input and a sensed current output, is connected through said bias input to at least one bit-line and is connected to said second terminal of each memory cell in said column associated with at lest one bit-line, comprising the steps of:

(a) applying a current signal on said bit-line;

(b) applying a voltage signal on said word-line, said application of said current signal to said bit-line and said voltage signal thereby addressing a memmory cell, wherein said addressed memory cell to pass current through said second terminal when a binary one is stored in said memory addressed cell, and wherein when a binary zero is stored in said memory cell, current is not passed through said second terminal; and

(c) sensing whether there is a change in current passing through said sensed current input to said sensed current output of said superconductor sensing means, wherein a change in the current indicates that a combination of current from said second terminal of said addressed memory cell and said bit-line is passing through and a binary one stored, and wherein no change in the current indicates that only current from the bit-line is passing through and a binary zero is stored.

32. A method of accessing from a memory cell having at least a first terminal and a second terminal information in binary forms of the type useful in computer or logic circuit applications, wherein a matrix comprised of a

plurality of memory cells of common design is formed in a row and column format, with rows being addressed via word lines, wherein each word line is connected to said first terminal of each memory cell in said row, and columns being addressed via bit-lines, wherein a superconducting current sensing means having a biased current circuit with a bias input and a bias output, and a sensed current circuit with a sensed current input and a sensed current output, is connected through said bias input to at least one bit-line and is connected to said second terminal of each memory cell in said column associated with at lest one bit-line, comprising the steps of:
(a) applying a current signal on said bit-line;
(b) applying a current signal on said word-line, said application of said current signal to said bit-line and said current signal to said word-line, thereby addressing a memory cell, wherein said current signal is passed to said second terminal of said addressed memory cell when a binary one is stored in said addressed memory cell and said current signal not being passed to said second terminal when a binary zero is stored; and
(c) sensing whether there is a change in current passing through said sensed current input to said sensed current output of said superconductor sensing means, wherein a change in the current indicates that a combination of current from said second terminal of said addressed memory cell and said bit-line is passing through and a binary one stored, and wherein no change in the current indicates that only current from the bit-line is passing through and a binary zero is stored.

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Document Number 2

Entry 2 of 3 File: USPT Nov 15, 1994

US-PAT-NO: 5365476
DOCUMENT-IDENTIFIER: US 5365476 A

TITLE: Three-port Josephson memory cell for superconducting digital computer
DATE-ISSUED: November 15, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mukhanov; Oleg A.	Rye Brook	NY	N/A	N/A

US-CL-CURRENT: 365/162; 326/3, 327/186, 327/527, 365/160

CLAIMS:

What is claimed is:
1. A method of storing data in a superconducting memory cell and retrieving the stored data, said memory call receiving a data input signal from a data line, a write enable signal from a write line, a first read enable signal from a first read line, and a second read enable signal from a second read line, said memory cell transmitting a first data output signal to a first sense line and a second data output signal to a second sense line, said method comprising the steps of:
opening a write gate in response to said write enable signal being received from said write line to divert and store said data input signal as a circulating current in said memory cell;
sensing said circulating current with a first read gate to generate said first data output signal, and transmitting said first data output signal from said memory cell to said first sense line in response to said first read enable signal; and
sensing said circulating current with a second read gate to generate said second data output signal, and independently transmitting said second data output signal from said memory cell to said second sense line in response to said second read enable signal, so that said circulating current can be sensed independently or simultaneously on said first sense line or said second sense line.

2. The method as claimed in claim 1, wherein said circulating current flows in series through a gated current path of said write gate, a control current path of said first read gate, and a control current path of said second read gate so that said circulating current is circulated in a single loop.
3. The method as claimed in claim 1, wherein a first portion of said circulating current flows in a first loop including a gated current path of said write gate and a control current path of said first read gate, and a second portion of said circulating current flows in a second loop including said gated current path of said write gate and a control current path of said second read gate.
4. The method as claimed in claim 1, wherein said first data output signal is transmitted from said memory cell to said first sense line by a first buffer gate in response to said first read enable signal being diverted by said first read gate to said first buffer gate when said circulating current is present; and wherein said second data output signal is transmitted from said memory cell to said second sense line by a second buffer gate in response to said second read enable signal being diverted by said second read gate to said second buffer gate said when said circulating current is present.
5. A superconducting memory cell, said memory cell receiving a data input signal from a data line, a write enable signal from a write line, a first read enable signal from a first read line, and a second read enable signal from a second read line, said memory cell transmitting a first data output signal to a first sense line and a second data output signal to a second sense line, said superconducting memory cell comprising a plurality of Josephson gates, said Josephson gates including:
a write gate having a control current path connected to said write line for receiving said write enable signal, and a gated current path connected to said data line for receiving said data input signal and storing said data input signal as circulating current in response to said write enable signal;
a first read gate having a control current path connected to the gated current path of said write gate for sensing said circulating current to generate said first data output signal, said first read gate having a gated current path connected to said first read line and said first sense line for transmitting said first data output signal from said memory cell to said first sense line in response to said first read enable signal; and
a second read gate having a control current path connected to the gated current path of said write gate for sensing said circulating current to generate said second data output signal, said second read gate being connected to said second read line and said second sense line for transmitting said second data signal from said memory cell to said second sense line in response to said second read enable signal.
6. The superconducting memory cell as claimed in claim 5,

wherein the gated current path of said write gate, the control current path of said first read gate, and the control current path of said second read gate are connected in series to form a single loop for conducting said circulating current.

7. The superconducting memory cell as claimed in claim 5, wherein the gated current path of said write gate, the control current path of said first read gate, and the control current path of said second read gate are connected in parallel to form two loops for conducting said circulating current.

8. The superconducting memory cell as claimed in claim 7, wherein said cell is formed on a planar substrate, and said circulating current circulates in a clockwise direction in one of said two loops and circulates in a counter-clockwise direction in the other of said two loops.

9. The superconducting memory cell as claimed in claim 5, wherein said write gate, said first read gate, and said second read gate are two-junction superconducting quantum interference devices (SQUIDs).

10. A superconducting memory cell, said memory cell receiving a data input signal from a data line, a write enable signal from a write line, a first read enable signal from a first read line, and a second read enable signal from a second read line, said memory cell transmitting a first data output signal to a first sense line and a second data output signal to a second sense line, said superconducting memory cell comprising a plurality of Josephson gates, said Josephson gates including:

a write gate having a control current path connected to said write line for receiving said write enable signal, and a gated current path connected to said data line for receiving said data input signal and storing said data input signal as circulating current in response to said write enable signal;

a first read gate having a control current path connected to the gated current path of said write gate for sensing said circulating current, said first read gate having a gated current path connected to said first read line for receiving said first read enable signal and diverting said first read enable signal when said circulating current is present;

a first buffer gate having a control current path connected to the gated current path of said first read gate for receiving said first read enable signal diverted from said gated current path of said first read gate when said circulating current is present, said first buffer gate having a gated current path connected to said first sense line for transmitting said first data output signal from said memory cell to said first sense line when said first read enable signal is diverted from said gated current path of said first read gate;

a second read gate having a control current path connected to the gated current path of said write gate for sensing said circulating current, said second read gate having a

gated current path connected to said second read line for receiving said second read enable signal and diverting said second read enable signal when said circulating current is present; and

a second buffer gate having a control current path connected to the gated current path of said second read gate for receiving said second read enable signal diverted from said gated current path of said second read gate when said circulating current is present, said second buffer gate having a gated current path connected to said second sense line for transmitting said second data output signal from said memory cell to said second sense line when said second read enable signal is diverted from said gated current path of said second read gate.

11. The superconducting memory cell as claimed in claim 10, wherein the gated current path of said write gate, the control current path of said first read gate, and the control current path of said second read gate are connected in series to form a single loop for conducting said circulating current.

12. The superconducting memory cell as claimed in claim 10, wherein the gated current path of said write gate, the control current path of said first read gate, and the control current path of said second read gate are connected in parallel to form two loops for conducting said circulating current.

13. The superconducting memory cell as claimed in claim 12, wherein said cell is formed on a planar substrate, and said circulating current circulates in a clockwise direction in one of said two loops and circulates in a counter-clockwise direction in the other of said two loops.

14. The superconducting memory cell as claimed in claim 10, further comprising a first resistor and a second resistor; wherein said first resistor, the gate current path of said first read gate, and the control current path of said first buffer gate are connected in series; and wherein said second resistor, the gated current path of said second read gate, and the control current path of said second buffer gate are connected in series.

15. The superconducting memory cell as claimed in claim 10, wherein said write gate, said first read gate, said second read gate, said first buffer gate, and said second buffer gate are two-junction superconducting quantum interference devices (SQUIDs).

16. The superconducting memory cell as claimed in claim 15, wherein said write gate, said first buffer gate, and said second buffer gate are symmetric SQUIDs; and wherein said first read gate and said first write gate are asymmetric SQUIDs.

17. The superconducting memory cell as claimed in claim 10, wherein said memory cell is included in a row of memory cells threaded by said write line, said first read line, and said second read line; and wherein said memory cell is included in a column of memory cells threaded by said data line, said first sense line, and said second sense line.

18. The superconducting memory cell as claimed in claim 17, wherein said write line is connected in series with the control current path of said write gate, said first read line is connected in series with the gated current path of said first read gate, said second read line is connected in series with the gated current path of said second read gate, said data line is connected in series with the control current path of said write gate, said first sense line is connected in series with the gated current path of said first buffer gate, and said second sense line is connected in series with the gated current path of said second buffer gate.

19. The superconducting memory cell as claimed in claim 10, wherein said cell includes no Josephson gates other than said write gate, said first read gate, said second read gate, said first buffer gate, and said second buffer gate.

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